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Equalizing the Use of Voltage Sources in Multi-level Structures

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Abstract:

In multi-level converters which employ several DC voltage sources to deliver an AC output waveform by voltage levels, the selection method and use time of each source has direct effect on the longevity of sources and consequently total system. It is obvious that equal entrance and exit of voltage sources and also time use of them, increase longevity of sources and total system. On the other hand, same condition of working in voltage sources, yield to same condition for switches and uniformed heat distribution produced due to power losses. In this paper the subject of equalizing the use of voltage sources in multi-level structures, especially in symmetrical CHB, would be discussed. For this purpose, switching tables of CHB is corrected and Simulation results on a seven level of this structure with both prevalent and proposed methods are presented. These results confirm performance of corrected switching table and shows improvement in proposed converter work and uniformity in power loss distribution created by switches.

Keywords: Multi-level converter, Equal Use of Sources in MLI, Monotonous Distribution of Power Loss, correction in switching table of symmetrical CHB

1. Introduction

In order to use distributed DC generation sources like solar cells using DC/DC converters is necessary due to changes in ambient conditions. This converter fixes generated voltage and provides it. The fixed DC voltage in some cases is used to feed local loads but in general they are used to connect to AC grid or feed AC loads with a DC/AC converter. Meanwhile DC/AC multi-level structures are used because of near waveforms to sinusoidal in comparison to other structures. There are several types of multi-level converters which NPC, CHB and Diode Clamped are the popular ones [1]. Also there are other types of multi-level converters which emphasis on some special features like reduction of elements [2-3], increase in efficiency of converters connected to PV cells [4-5], omit the grid connected transformer [6-9], reduction of switch stress [10] and other features which are proposed in such papers.

Multi-level structures employ several DC voltage sources to build an AC output which the selection method and order of the use of each source regard to the number and time use of them and it affects sources and whole system. Multi-level converters are divided into two symmetrical and asymmetrical groups due to the amplitude of voltage sources. In symmetrical category, amplitude of all voltage sources is the same while in asymmetrical it is not the true [3]. In asymmetrical multi-level converters, in order to build intended output

voltage level, amplitude of each voltage source is set separately. In this paper the concept of "equal use of voltage sources in multi-level structures" is introduced and the ability of equalization of the use of sources in symmetrical CHB structure is analyzed.

2. Prevalent method of the use of voltage sources

In multi-level structures by using several DC voltage sources and special order of switching, which usually can be defined through table, output voltage is obtained. This set of switching is implemented to achieve output voltage level near to sinusoidal waveform with the lowest harmonic distortion. It is completely obvious that equal condition of DC source implementation, results uniformity in their status and increases the beneficial longevity of sources. In n level structure, each cycle of output waveform is built by using m sources which the relationship between n and m can be declared through (1).

$$m = \frac{n-1}{2} \tag{1}$$

In a half cycle and with considering no zero level, the number of achievable levels is equal to the number of sources. For simplicity voltage levels are named by separating positive half cycle into two increasing part (between zero to 90 degrees) and decreasing part (between 90 to 180 degrees). As it can be seen from Fig.1, voltage levels in increasing part are name 1 to m and in decreasing part are named from m to 1' with considering their symmetry. Here, levels of increasing part are denoted by number and levels of decreasing part are specified by primed numbers respectively.

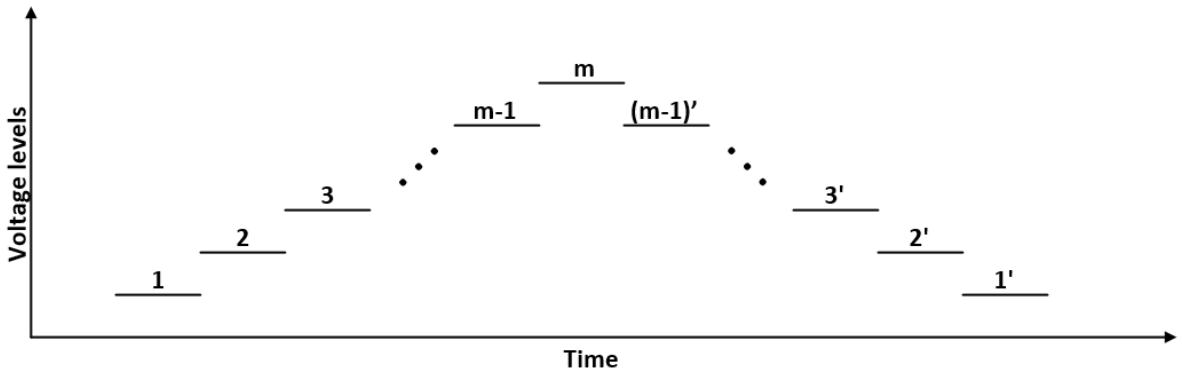

Fig1: Generated Voltage levels by a n level converter in positive half cycle

Table.**1**: Prevalent method of source implementation in positive half cycle

Used voltage sources	Output voltage	level
V_1	V	1, 1′
V_1+V_2	2V	2, 2′
$V_1+V_2+V_3$	3V	3, 3′
$V_1+V_2+V_3+\ldots+V_{m-1}$	(m-1)V	(m-1) , (m-1)′
$V_1+V_2+V_3+\ldots+V_{m-1}+V_m$	mV	m

Table.1 shows the prevalent method of the use of sources for building each voltage level and also shows the resultant output voltage. Based on this table, for building same voltage levels, in both increasing and decreasing part similar sources are used. Equation (2) gives the number of the use of source k in prevalent method.

$$t=m-k+1 \quad (2)$$

In this equation, k is a specified number given to the source, m is total sources of multi-level converter and t is considered the total times of the use of source. Based on Fig.1, number of levels of n level waveform which is built by m sources and in one half period, with considering zero level, can be found by (3).

$$s=2.m \quad (3)$$

By assuming T as switching period, time duration for each level (t_s) is calculated from (4).

$$t_s = \frac{T}{2s} = \frac{T}{4m} \quad (4)$$

By defining time duration of each level and number of levels which each source contributes to build them, the implementation time of each source can be calculated by (5).

$$T_m=s.t_s \quad (5)$$

In Table.2 number of contributions and time duration of each source are shown which based on this table number and time duration of the use of sources are not as same as each other and are totally different. In this table contribution of each source for building levels are shown. By looking at this area, V_1 contributes for building all levels while V_m is used only to build the highest level.

Table.2: Number of contribution and time duration of sources in prevalent method to build half cycle output voltage

Number of contributions to build voltage levels (t)	Use time (t_m)	Levels	Sources
m	$(2m-1)t_s$	1 to 1′	V_1
m-1	$(2m-3)t_s$	2 to 2′	V_2
m-2	$(2m-5)t_s$	3 to 3′	V_3
m-k+1	$(2m-2k+1)t_s$	k tok′	V_k
2	$3t_s$	(m-1) to (m-1)′	V_{m-1}
1	t_s	Just m	V_m

Table.3: Proposed method for use of sources in positive half cycle

Used voltage sources	Output voltage	Levels
V_1	V	1
V_1+V_2	2V	2
$V_1+V_2+V_3$	3V	3
$V_1+V_2+V_3+\ldots+V_{m-1}$	(m-1)V	(m-1)
$V_1+V_2+V_3+\ldots+V_{m-1}+V_m$	mV	m
$V_2+V_3+\ldots+V_{m-1}+V_m$	(m-1)V	(m-1)′
$V_3+\ldots+V_{m-1}+V_m$	3V	3′
$V_{m-1}+V_m$	2V	2′
V_m	V	1′

3. The proposed equivalent use of sources method

In order to equalize the number of sources contributed in building voltage levels and the time duration of their use, Table.1 must be corrected and like Table 3, voltage sources be used. In this table, for building level one, source V_1 has been used and for building level two source V_2 is added to V_1. Levels 3 to m are built by adding sources V_3 to V_m respectively. But in increasing levels, in comparison to prevalent method, reduction in sources starts from source V_1. In another word for building level (m-1)' instead of omitting V_m itself, source V_1 is omitted. In this method, source V_1 which was used in all increasing levels in prevalent method, now is just used to construct increasing levels. Due to the corrected table, for building decreasing levels, V_m is replaced by V_1 and instead of contribution in one level, it is used in m levels. Other sources are used to construct m levels with this method.

Based on the proposed method in table 3, each source is used m times. For example source V_1 is used for building level 1 to m which it means it is used m times and the total time of using that, is mt_s. Source V_2 is used to build level 2 to (m-1)' and it has same situation of source V_1.

Table 4 shows the number of contribution or in fact the number of levels that each source has used to build by proposed method. Respect to this table, number of contributions and

time duration of all sources are the same and the use of each source is shown in the Table where it is different from prevalent method.

Table 4: Contribution number and duration time of sources in proposed method for building a half cycle voltage

Times of contribution to build voltage levels (t)	Use time (t_m)	Levels	Source
m	mt_s	1 to m	V_1
m	mt_s	2 to (m-1)′	V_2
m	mt_s	3 to (m-2)′	V_3
m	mt_s	k to (m-k+1)′	V_4
m	mt_s	(m-1) to 2′	V_{m-1}
m	mt_s	m to 1′	V_m

Here by moving and optimal distribution of sources for building levels, the necessary conditions for equalizing the use of each source and its time duration becomes possible. In next section a symmetrical seven level CHB is simulated with both prevalent and proposed method and results are compared.

4. Implementation of proposed method on CHB Structure

To validate the subjects, n level CHB structure with m DC sources, is assumed. Fig.2 shows m base unit and positive, zero and negative outputs. Table.6 shows the prevalent method of the use of voltage sources to build half positive output cycle. In this table, HB_t means t base unit which consists of Voltage source t and a bridge structure. Based on this table, Unit HB_1 is used to build all m output voltage levels, while unit m (HB_m) is used just only one time and it is when building highest voltage level (m). As it can be seen from table, number and time duration of voltage sources is not equal and consequently depreciation and heat dissipation of switches in units does not have uniform distribution.

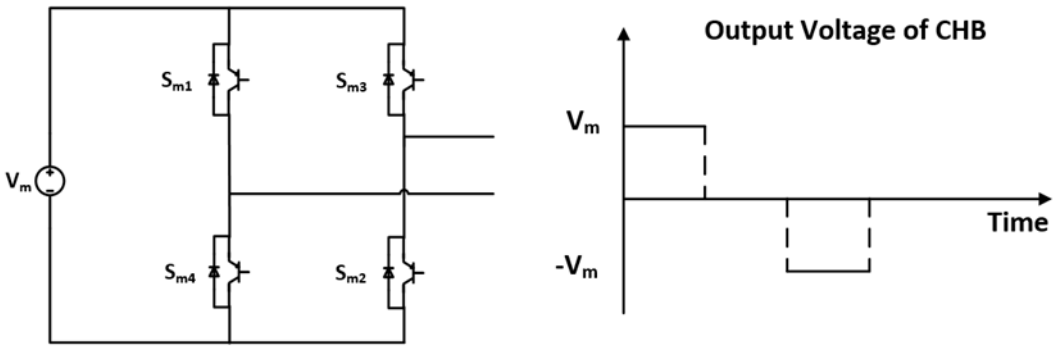

Fig 2: Number m unit, method of numbering of related switches and output voltage waveform

Table 5: Prevalent method used to select voltage sources in CHB structure for half positive cycle

Used sources	HB_m	HB_{m-1}	HB_{m-2}	HB_3	HB_2	HB_1	level
V_1	0	0	0	0	0	1	1
V_1+V_2	0	0	0	0	1	1	2
$V_1+V_2+V_3$	0	0	0	1	1	1	3
$V_1+V_2+V_3+\ldots+V_{m-1}$	0	1	1	1	1	1	m-1
$V_1+V_2+V_3+\ldots+V_{m-1}+V_m$	1	1	1	1	1	1	m
$V_1+V_2+V_3+\ldots+V_{m-1}$	0	1	1	1	1	1	(m-1)′
$V_1+V_2+V_3$	0	0	0	1	1	1	3′
V_1+V_2	0	0	0	0	1	1	2′
V_1	0	0	0	0	0	1	1′

In proposed method, in addition to equalization in the use of time and number of voltage sources it is attempted to have a monotonous distribution of power loss in switches. For implementation of these demands, to build positive half cycle, by using such base units, entrance and exit of each unit is proposed base on Table 6. In Table 6, level 1 is built by V_1 and next level can be built by adding V_2 to V_1. Next levels of positive half cycle can be built by adding voltage sources in such way. Until this step, all steps are same as prevalent method. But to build decreasing levels in positive half cycle or m to 1' instead of omitting voltage sources by the order of V_m to V_1, an opposite order or V_1 to V_m is used. This change in order, yields to equalization in time and number of the use of the voltage sources and the number of use of sources is same for all of them and equals to m.

5. Power loss comparison

Power loss in converters consists of conduction loss and switching loss and can be found by (6) and (7):

$$P_{cound} = R_{on} I_{on}^2 \tag{6}$$

$$P_{sw} = \frac{t_{sw,off} + t_{sw,on}}{2} f_{sw} V_{off} I_{on} \tag{7}$$

In (6), R_{on} is resistance and I_{on} is the current passing through switches when they are on. In (7) f_{sw} is switching frequency, $t_{sw,on}$ and $t_{sw,off}$ are time of operation of switches in on and off mode respectively and V_{off} is drain-source voltage of MOSFET in off state. The comparison is done by choosing same structure, same switches and equal current and voltage of the load for converter. In this manner, because of same R_{on} and I_{on}, conduction power loss in both methods is unchanged. In switching power loss all quantities are the same but operating frequency must be analyzed.

Table 6: Implementation of proposed method of the use of voltage sources in CHB structure for positive half cycle

Used sources	HB_m	HB_{m-1}	HB_{m-2}	HB_3	HB_2	HB_1	Level
V_1	0	0	0	0	0	1	1
V_1+V_2	0	0	0	0	1	1	2
$V_1+V_2+V_3$	0	0	0	1	1	1	3
$V_1+V_2+V_3+\ldots+V_{m-1}$	0	1	1	1	1	1	m-1
$V_1+V_2+V_3+\ldots+V_{m-1}+V_m$	1	1	1	1	1	1	m
$V_2+V_3+\ldots+V_{m-1}+V_m$	1	1	1	1	1	0	(m-1)′
$V_{m-2}+V_{m-1}+V_m$	1	1	1	0	0	0	3′
$V_{m-1}+V_m$	1	1	0	0	0	0	2′
V_m	1	0	0	0	0	0	1′

Due to Table 5, it can be seen that in the prevalent method to build one half cycle, each unit is used only one time. Also Table 6 shows the same condition of proposed method for units. The only difference is time duration of the use of each unit which has an equalized distribution in proposed method. So the switching frequency and power loss due to it, in both methods are the same. As it was mentioned before, one of the advantages of proposed method is the equalization of time duration of the use of voltage sources which yields to partly monotonous distribution of conduction loss of switches and prevents from heat centralize in one or more units because of lower presence time of unit. As a result by using this method, time duration of units become equalized and power loss doesn't change.

6. Stress voltage on switches

In symmetric structure of CHB, voltage stress (V_{st}) is calculated from (8)

$$V_{st}=2(n-1)V \tag{8}$$

In this equation n refers to number of levels, V is voltage of sources. It is clear that because of no change in structure and switches type, voltage stress in both methods are the same.

7. Comparison between prevalent and proposed methods in symmetrical seven level CHB

Unit number m or HB_m consists of 4 switches which the way of their numbering is shown on Fig. 2. In this numbering method, subtitle is composed of two numbers which first digit from right is the switch number of related unit and second digit is the number of unit. Here for showing the concepts, a symmetrical seven level CHB is employed.

Output waveforms or load voltage is shown on Fig 3. For simplicity in comparison and because of similarity between positive and negative half cycles on the output in both methods, simulation results are shown only for positive half cycle.

Given that the number of voltage sources or m=3, number of levels and time duration of each level of this converter in positive half cycle can be found by (9) and (10).

$$S=2m=6 \tag{9}$$

$$t_s = \frac{T}{2s} = \frac{T}{4m} = \frac{0.02}{12} \tag{10}$$

In Fig.4 switching pulses for implementation of proposed method are shown. Based on it, switching is done such a way that time duration of on state of switches is not the same. i.e. switches S_{12} and S_{32} in five levels and switches S_{13} and S_{32} only in one level are in on mode from positive half cycle. It is obvious that with this condition, conduction power loss in theses switches is not the same and produced heat is not distributed as well.

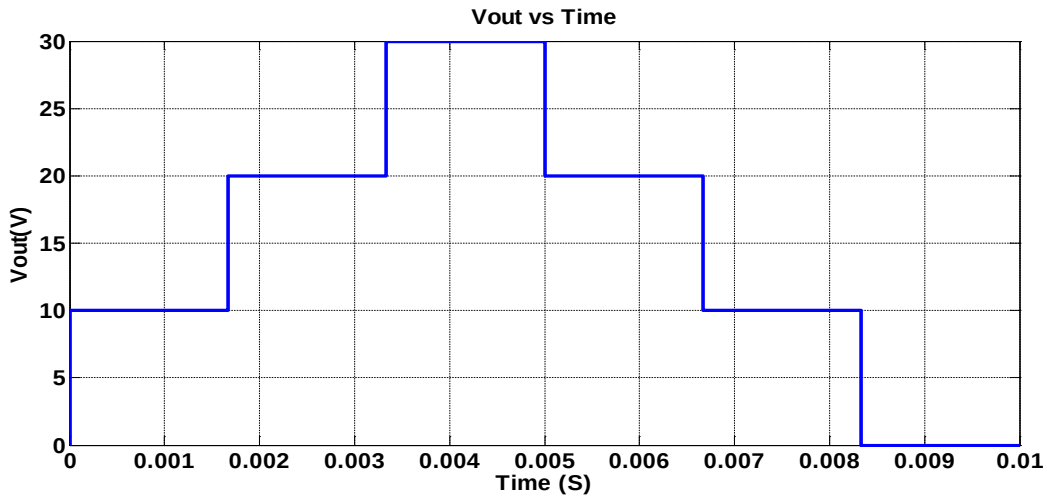

Fig 3: Output resultant voltage with both prevalent and proposed methods in a symmetrical seven level CHB

In Fig 5. necessary pulses for implementation of proposed method are shown. Based on this figure switches S_{12}, S_{13}, S_{22}, S_{23}, S_{33} in three levels or positive half cycle are on, which in comparison to prevalent method, conduction time in these switches become same and consequently produced heat from conduction power loss has a monotonous distribution. In both prevalent and proposed methods, switches S_{11},S_{21} and S_{31} conduct in all positive half cycles and switches S_{14},S_{24} and S_{34} are in off state. So because of no change in status of former switches, there is no impact on power losses. In each unit, switches number 3 (S_{13}, S_{23} and S_{33}) and number 4 (S_{34}, S_{24} and S_{14}) put negative voltage on output and then it is expected that they be completely open in positive half cycle.

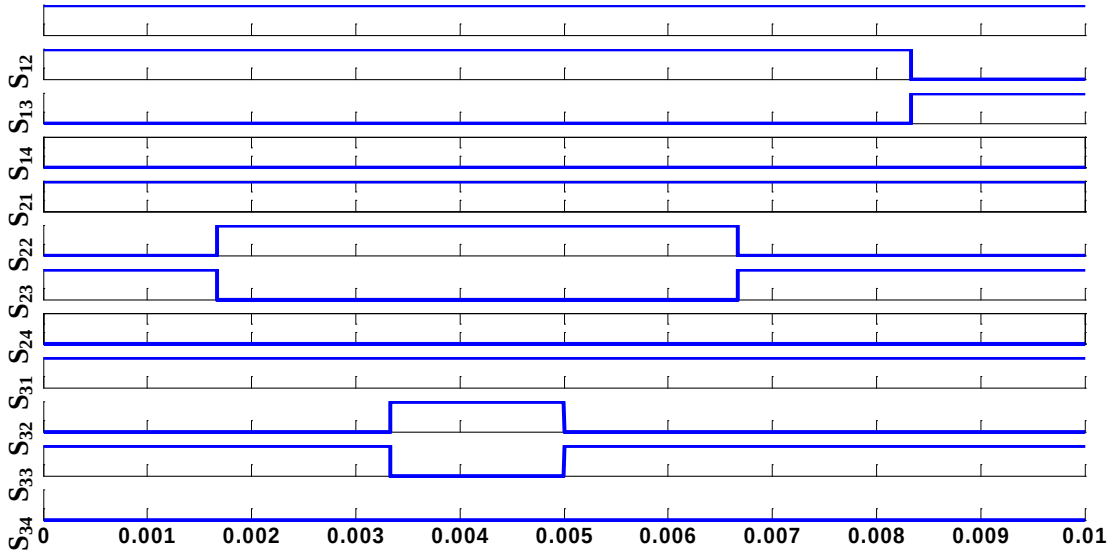

Fig 4: Gate pulses of switches in implementation of prevalent method for a symmetrical seven level CHB

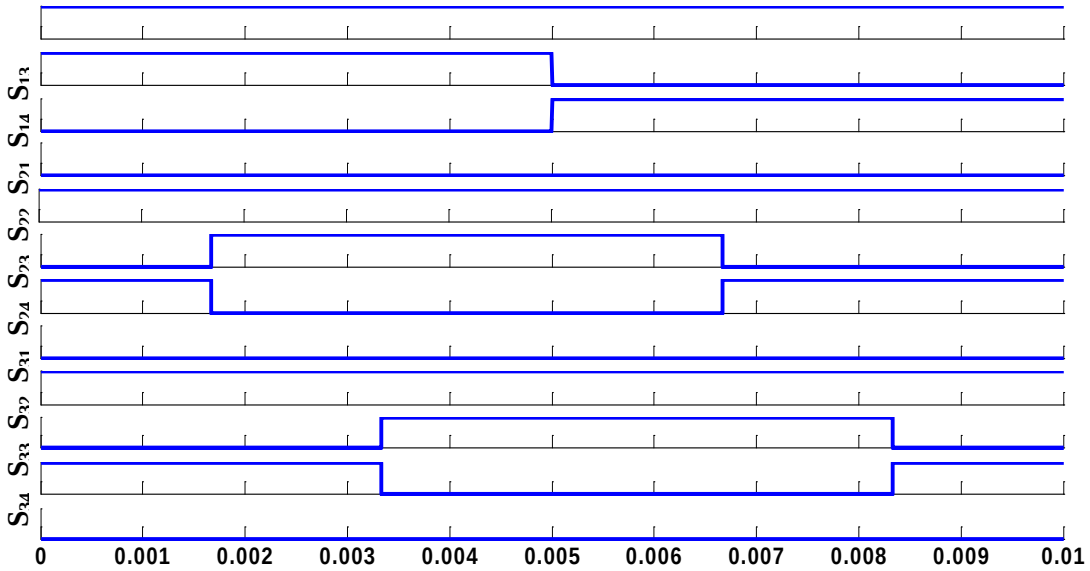

Fig 5: Gate pulses of switches in implementation of proposed method for a symmetrical seven level CHB

As it can be seen, this problem is true for both switches except switches number 3, because of contribution in building zero level, like switches number 4 are not completely off. Also zero level can be built by two couples of first and third or second and forth switches. But this subject must be managed to have minimum numbers of switching through turning switches on before zero level happens. In another word, for building every zero state, closed switches in previous state should be paid attention and by closing only one switch, zero level must be built. In Fig.6 the entrance and exit time of sources V_1 to V_3 in implementation of prevalent method are shown.

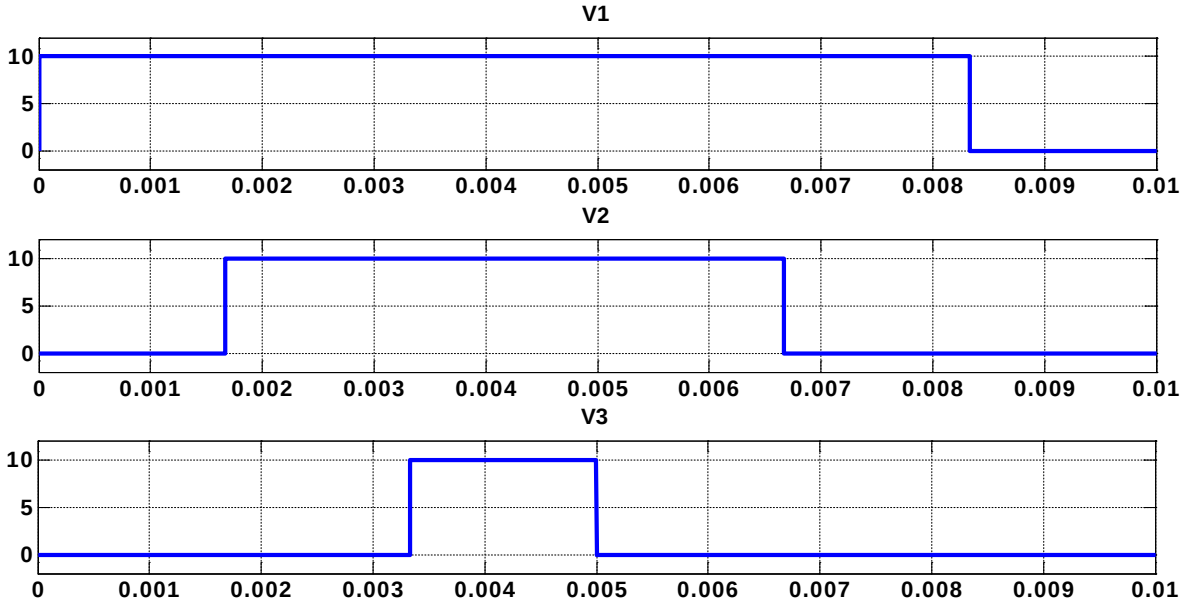

Fig 6: Usage time of switches for implementation of prevalent method for a symmetrical seven level CHB

Based on these diagrams, number of the use of voltage sources is equal but time duration of their use is not equal. In this method, voltage source V_1 during 5 levels, V_2 during 3 levels and V_3 during one level contribute in building output waveform for a positive half cycle. Fig.7 shows the diagrams of the use of voltage sources by the mean of proposed method. Based on this figure by implementation of proposed method, in addition to numbers of the use, time of the use is the same and would be equal to three levels or a positive half cycle.

8. Conclusion

The purpose of this paper is equalization of number and time of the use of the voltage sources in symmetrical multilevel converter. By analysis of the output waveform configuration and structure of these constructions, it can be seen that it is possible to build the same output with equal condition of the use of sources. In addition to equal distribution of power loss of switches and produced heat, equally use of voltage sources result in depreciation uniformity of sources. To achieve mentioned goals, a method is proposed which there is no need to change structure of converter and it is just by changings in implemented switching time. So it is expected that by implementing switching based on proposed table, voltage stress on switches and number of switching times remain the same. Results of simulation on a symmetrical seven level CHB, with implementation of both prevalent and proposed methods confirm the above explanations.

Also the comparison between simulated results show that by equalizing number and time of use of voltage sources, there is no change in number of switching so power losses never happen. On the other hand, voltage stress doesn't change respectively. This method, equalizes the time of the use of switches and consequently distribution of power loss becomes monotonous.

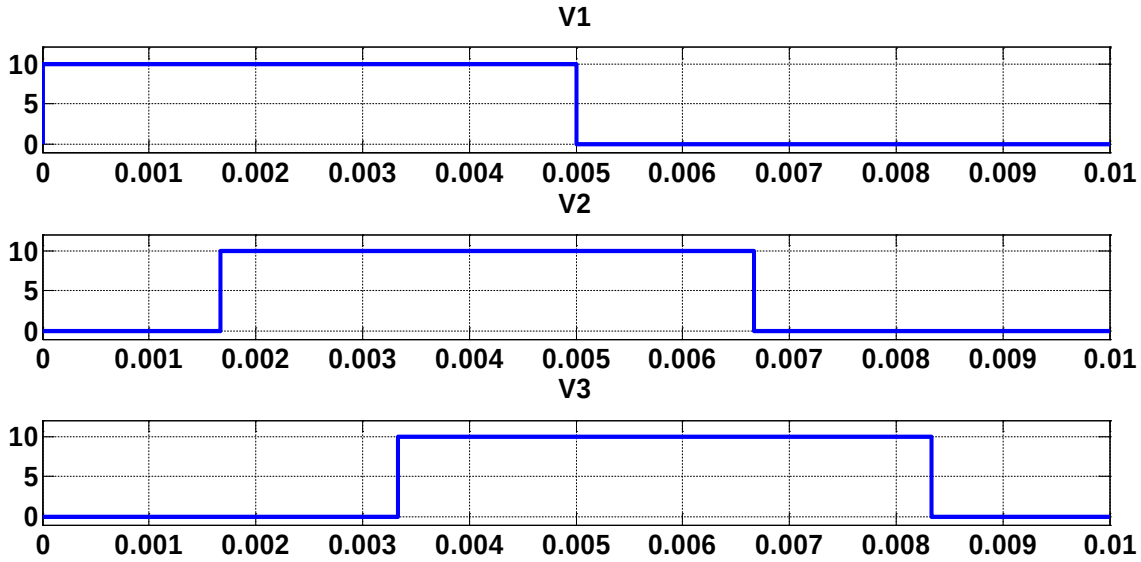

Fig 7: Time durations of the use of sources in implementation of proposed method on a symmetrical seven level CHB

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