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Designing Voltage-Controlled Oscilltor using Novel hybrid method

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Abstract

This paper, in line with modern telecommunication development, investigates controlled-oscillator design and simulation, i.e. central nuclear of telecommunication systems synthesis. In this paper, useful frequency oscillations required by controlled oscillator are designed and provided via voltage applying consisting tune control, reactor diode and digital words, and efficient results were obtained. Designing and simulation of oscillator using negative resistance with self, capacitor and inductors as capacitor tank of inductor to cause positive feedback and oscillation volatility. In order to make negative resistance from active elements i.e. transistors, due to lower occupation and applicability on low power ICs. Required negative resistance simulated by pairing cross transistors. Capacitor bank including transistor capacitor (Gate source) oscillators where designed and simulated in 0.180 um size with CMOS technology by ADS software. The results are summarized in a table so that designed merit value is199dBc/Hz and indicating the design quality. The obtained phase noise from simulation of voltage-oscillator with voltage equals 146dBc/Hz and indicating the frequency spectrum purity. Central frequency of the 2.42 GHz and the offset of calculation and criterion formula merit is 1 MHz. power consumption is below 3 mv.

Keywords: Voltage-controllable Oscillator, fracture criteria, negative resistance, capacitor bank, cross couple.

1. Introduction

In past few decades and following integrated circuit invention, human life has experienced a great revolution. The technology, during few past decades and through fast development, made it plausible to create more complex systems with low prices, in small dimensions, and higher speed. Telecommunication industry has experienced daily growing, while in past decade the exponential growth provided increased usage of the systems while exponential use of the technology devoted to more than 5 billion people though the world, i.e. 80 percent of the world population. Variety of telecommunication products such as cell phones, local wireless networks, GPS, high frequency detection system, wide broadband,… in most places in the world considered as inseparable part of human daily life. It is almost impossible to imagine a world without cell phones.

In most references, noise reduction of oscillators considered as main goal of the study and maneuver point for researchers, reduction of power consumption and construction space considered as next issues. As mentioned above, it is in contrary to phase noise and it is not possible to promote both of them simultaneously.

It is worth to mention that most work and references consider central frequency as the most important one, and achieving better phase noise in frequencies considered the least, it means that higher frequency works has complexities and difficulties. Another issue that other work focus on it is tune range, which is an applied parameter in the designs, the wider tune range with small steps and high quality will be quality-controlled oscillator. This section reviews the papers to clarify the studies process in voltage controllable-oscillator. All papers and thesis that are reviewed, focus mostly on phase noise reduction, so that the mentioned factors are common between the studies and comparison of oscillators

Considering a paper that the author focus on filtering and attracting the noise effects elements in filter design, then optimized the design due to noise factors difficulties of filter design.

Noteworthy point is that no one discussed removing and absorption of basis effects of structures since significant effect play crucial role in pads function and noise reduction, this approach may be considered as well In a reference of feedback acts utilized to optimize controllable oscillator, so that in proposed circuits capacitors created feedback route which is not only a feedback route but also noise problems of structures of current self in the gate route is smoother couple cross to promote the phase noise. The numbers of Self in DC currency, by itself can reduce de-charge capacitor bank and reference noises, however the task is plausible. This task considered as disadvantage , if DC self size is not selected appropriately, it means that frequency tune are accessible with big steps, while we attempt to have wide frequency range with following steps:

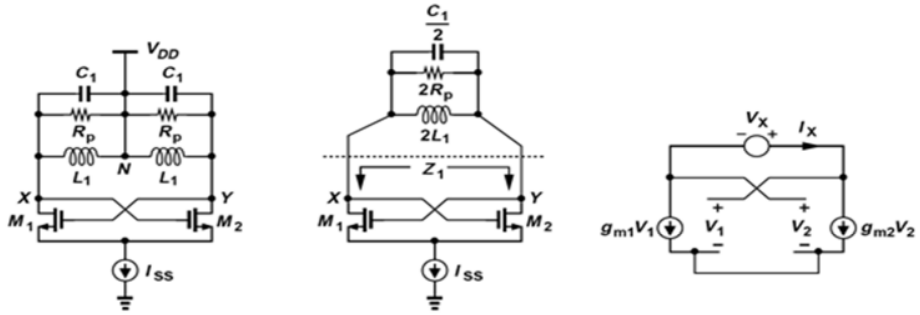

Figure 1: Oscillator with negative active

$$I_x = -g_{m1}V_1 = g_{m2}V_2 \tag{1}$$

$$\frac{V_x}{I_x} = -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right) \tag{2}$$

$$for g_{m1} = g_{m2} \Rightarrow \frac{V_x}{I_x} = \frac{-2}{g_m} \tag{3}$$

For designing and simulating negative resistance approach with self and capacitors considered as self capacitor tank – causing positive feedback and efficient oscillation. For creating negative oscillation from active elements i.e. transistors, were used due to lower occupation volume implementation capability on low-power ICs. Required negative resistance by couple binding of transistors were designed and simulated, as indicated in the figure. Capacitor bank comprises transistor capacitors (source gate capacitor). Being control with control words –FWC feature is

due to cover comprehensive control of frequency bandwidth. It has voltage controlled oscillator. In order to cover total bandwidth Binary and Fibinacci weighting were used and they were seen in some papers. Here, we use binary weighting that meet efficient goal of paper design Digital word FWC utilized for capacitor control, so that conditioning digital word=1 , then capacitor capacity is 0C, while digital word is rational 0 , capacitor capacity will be +ΔC0C. Subscale k in the relation reflecting capacitor weight position in the system and binary weighting.
K=0 , capacitor weight =102 and k=1 the capacitor weight =212, and follows in binary system. Following equation indicates capacitor bank of designed oscillator in the paper

$$C_{binery} = \sum_{k=0}^{N-1} C_{k_b} = \sum_{k=0}^{N-1} \left(C_{0,k_b}.2^k + \overline{FCW_{k_b}} \Delta C_{k_b}.2^k \right) \quad (4)$$

2. Findings

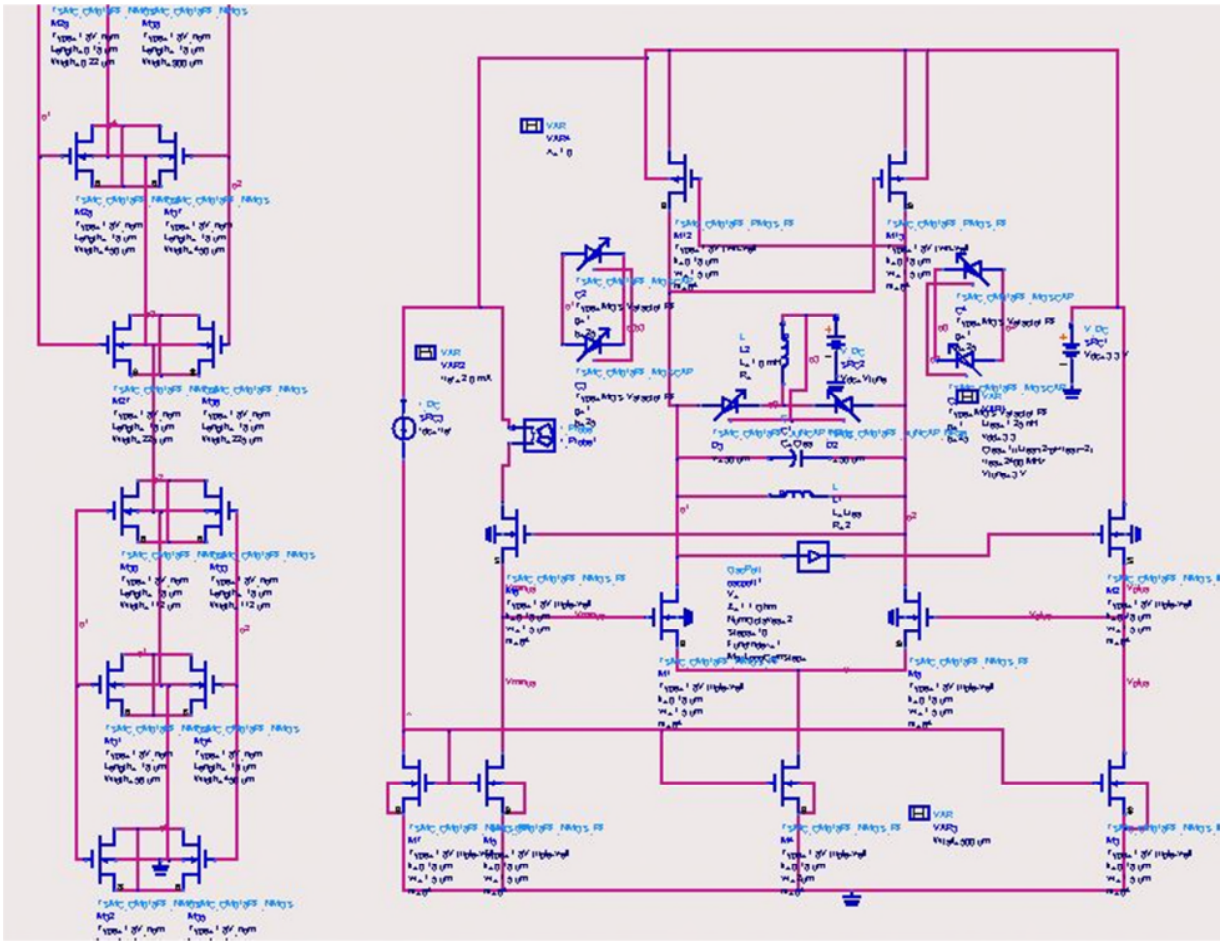

Figure 2: General view of designed oscillator

Figure 2 shows general view of voltage-controlled oscillator. The circuit composes capacitor bank, diode, negative resistance transistor reactors, circuit source, capacitor self tank, and every one play its role to have sinus output signal with frequency control capability.

The circuits designed so that have minimum power consumption while low power circuits design has higher priority in telecommunication circuits. Designing and simulation of transistor circuits CMOS RF ʌ micrometer, 0.18 micrometer i.e. minimum transistor length may be 0.18.
Capacitor simulation results in ADS software with voltage in 0.18 um CMOS technology provided with w=0.3 u and =0.18 um l values and n, p channels, indicatin capacitor capacity 320 aF to 580 aF.

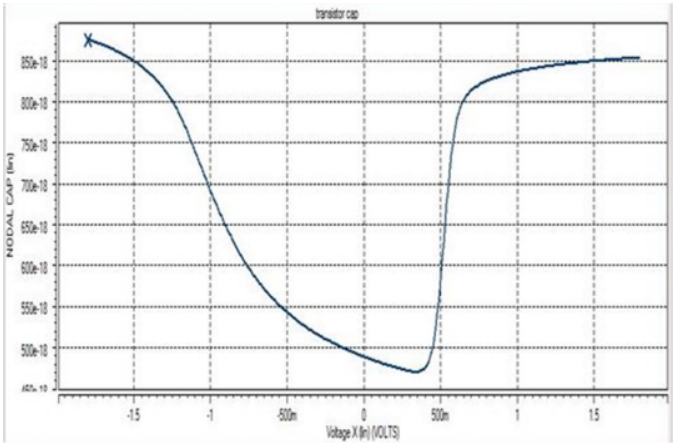

Figure 3: Swing capacitor with 0.18 umCMOS voltage ad w=0.3 u and l =0.18 um and n channel

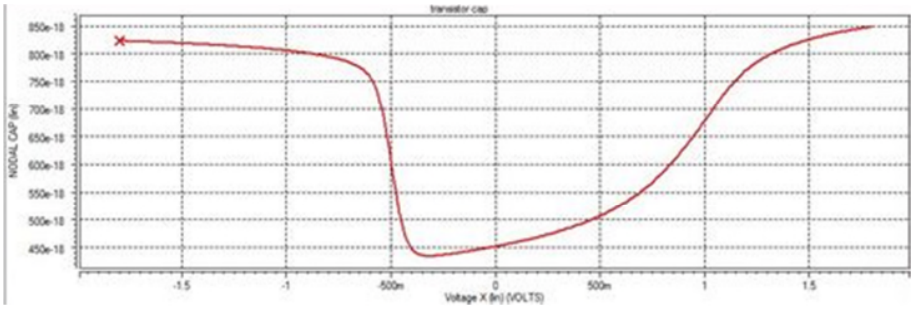

Figure 4: Swing capacitor with 0.18 umCMOS voltage ad w=0.3 u and l =0.18 um and p channel

This paper focuses on frequency alteration with voltage tune, the voltage tune value is applied when diodes and reactors, used as variable capacitor in this paper, to create variable frequencies with voltage, the changes are small and continous, so that resolution control voltage is tiny, output frequency will be smoother and tiny.

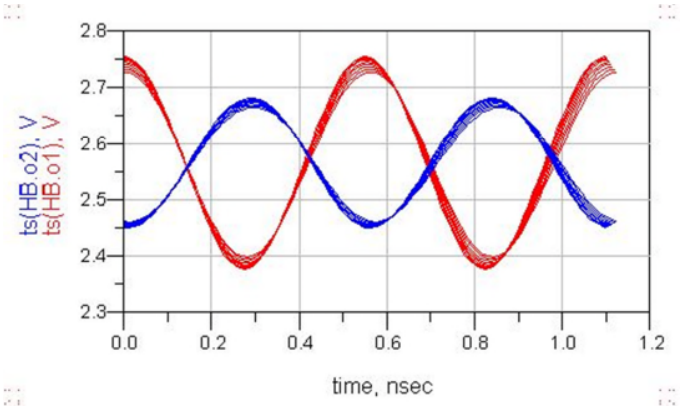

Figure 5: Oscillator output voltage in time scope

Phase noise graph provided with dBc/Hz. This unit reflects the concept that to what extent the output figure gets away when from central frequency getting away from central frequency is called frequency offset.

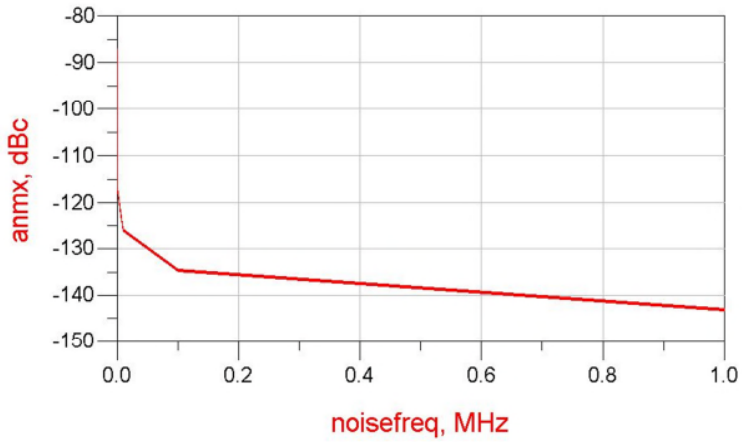

Figure 6: Phase noise graph observed in voltage-controlled oscillator

A crucial parameter in expression of voltage-controlled oscillator merit so that the higher absolute value, i.e. low phase noise (due to negative sign) the better merit criteria

$$FOM = 10\log\left[\left(\frac{fo}{\Delta f}\right)^2 * \frac{1}{P}\right] - (NF) \qquad (5)$$

That PN oscillator phase noise, P oscillator power consumption, (Δf) frequency offset from central frequency oscillator, fo, central frequency of oscillator

3. Discussion and conclusion

We obtained good results by designing and simulation of voltage-controlled oscillator, composed of tune control and diode reactor and digital word in the previous section. In this section earlier works are analyzed and compared comprehensively to provide the literature. Oscillator in 0.18 um in CMOS technology designed and simulated via powerful ADS software.

Obtained results and comparisons provided in comparison table, so that merit number of designed circuit is 146dbc/Hz reflecting good spectral purity value.

Table 1: comparing the results with other things vco design

Reference	Frequency (GHz)	Phase noise (dbc/Hz)	Technology (um)	Power (mw)	FOM (dbc/Hz)
This work	2.42	-146	0.180	3	-199
[1]	1.96	-125	0.350	1.87	------
[2]	56	-89	0.180	43	-168
[3]	2.4	-117	0.180	10	-175
[4]	40	-108.5	0.180	6	-193
[5]	4.84	-125	0.180	3.5	-190
[6]	1.88	-126	0.180	2.8	-193

It`s worth to mention that power consumption in different parts of voltage-controlled oscillator shall be investigated, in the thesis the most power consumption is used for the oscillator`s main transistor bias , then it had the currency resources and capacitor bank had the minimum power consumption.

Table 2: Values can be used for power consumption

Capacitor bank	Oscillator nuclear	Currency sources	Voltage-controlled oscillator parts
0.3	2	0.7	Power consumption mw

This thesis focus on reduction of power consumption and controlled-oscillator phase noise, the novelty of the work is combining two capacitor banks, reactor diode, and typical reactor in voltage-controlled oscillator, while increasing frequency tune and its limitation, however, extra low power consumption of capacitor bank reducing phase noise

Reduction of power consumption using central nuclear voltage-controlled transistors provide the best function with minimum currency. A suggestion is changing capacitor bank structure and weighting. Another one is changing diode numbers and utilized reactors shall be studied and simulated in future works. Another suggestion is miniature out the utilized technology or using novel ones in future works.

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